HIGH WIREABILITY MICROVIA SUSTRATE

ABSTRACT OF THE DISCLOSURE

The escape of signals from a semiconductor chip to a printed wiring board in a flip chip/ ball grid array assembly is improved by repositioning the signals from the chip through the upper signal layers of the carrier. This involves fanning out the circuit lines through the chip carrier from the top surface that communicates with the chip, through the core to the bottom surface where signals exit the carrier to the printed wiring board. This fanning out is achieved by making better utilization of the surface area of the signal planes between the core and the chip. The signals are fanned out on each of the top signal planes so that many more of the signals are transmitted through the vias in the core to the bottom signal planes where they can escape outside of the footprint area of the chip thereby increasing the density of circuits escaping the footprint area.